SDLS083

MARCH 1974-REVISED MARCH 1988

'246, '247, 'LS247 feature 'LS248 feature

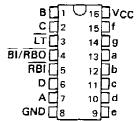
- Open-Collector Outputs Drive Indicators Directly
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

- Internal Pull-Ups Eliminate Need for External Resistors
- Lamp-Test Provision
- Leading/Trailing Zero Suppression
- All Circuit Types Feature Lamp Intensity Modulation Capability

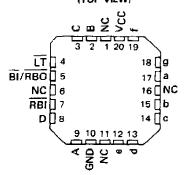
	†	DRIVER O	UTPUTS		TYPICAL	
TYPE	ACTIVE LEVEL	OUTPUT CONFIGURATION	SINK CURRENT	MAX VOLTAGE	POWER DISSIPATION	PACKAGES
SN54246	low	open-collector	40 mA	30 V	320 mW	J,W
SN54247	low	open-collector	40 mA	15 V	320 mW	J,W
SN54LS247	low	open-collector	12 mA	15 V	35 mW	J,W
SN54LS248	high	2-kΩ pull-up	2 mA	5.5 V	125 mW	J,W
SN74246	low	open-collector	40 mA	30 V	320 mW	J,N
SN74247	low	open-collector	40 mA	15 ∨	320 mW	J,N
SN74LS247	low	open-collector	24 mA	15 V	35 mW	J,N
SN74LS248	high	2-kΩ pull-up	6 mA	5.5 V	125 mW	N,L

SN54246, SN54247 . . . J PACKAGE SN54LS247 THRU SN54LS248 . . . J OR W PACKAGE SN74246, SN74247 . . . N PACKAGE SN74LS247, SN74LS248 . . . D OR N PACKAGE

(TOP VIEW)



SN54LS247, SN54LS248 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

description

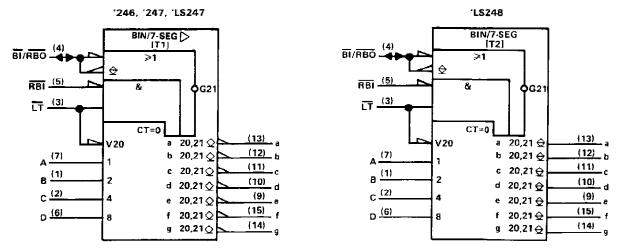
The '246 and '247 are electrically and functionally identical to the SN5446A/SN7446A, and SN5447A/SN7447A respectively, and have the same pin assignments as their equivalents. The 'LS247 and 'LS248 are electrically and functionally identical to the SN54LS47/SN74LS47 and SN54LS48/SN74LS48, respectively, and have the same pin assignments as their equivalents. They can be used interchangeably in present or future designs to offer designers a choice between two indicator fonts. The '46A, '47A, 'LS47, and 'LS48 compose the \Box and the without tails and the '246, '247, 'LS247, and 'LS248 compose the \Box and the \Box with tails. Composition of all other characters, including display patterns for BCD inputs above nine, is identical. The '246, '247, and 'LS247 feature active-low outputs designed for driving indicators directly, and the 'LS248 features active-high outputs for driving lamp buffers. All of the circuits have full ripple-blanking input/output controls and a lamp test input. Segment identification and resultant displays are shown below. Display patterns for BCD input counts above 9 are unique symbols to authenticate input conditions.

All of these circuits incorporate automatic leading and/or trailing-edge zero-blanking control (\overline{RBI} and \overline{RBO}). Lamp test (\overline{LT}) of these types may be performed at any time when the $\overline{BI}/\overline{RBO}$ node is at a high level. All types contain an overriding blanking input (BI) which can be used to control the lamp intensity by pulsing or to inhibit the outputs. Inputs and outputs are entirely compatible for use with TTL logic outputs.

Series 54 and Series 54LS devices are characterized for operation over the full military temperature range of -55 °C to 125 °C; Series 74 and Series 74LS devices are characterized for operation from 0 °C to 70 °C.



logic symbols†



 $^{^\}dagger$ These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, N, and W packages.

'246, '247, 'LS247 FUNCTION TABLE (T1)

DECIMAL OR			INP	UTS			BI/RBO†			o	UTPU	rs			NOTE
FUNCTION	LT	RBI	D	С	В	A		a	ь	c	d	e	f	9]
0	H	н	L	L	L	L	Н	ON	ON	ON	ON	ON	ON	OFF	
1	н	×	L	L	L	н	Н	OFF	ON	ON	OFF	OFF	OFF	OFF	
2	н	×	L	L.	н	L	н	ON	ON	OFF	ON	ON	OFF	ON	
3	н	Х	L	L	H	Н	H	ON	ON	ON	ON	OFF	OFF	ON	
4	Н	×	L	Н	L	L	н	OFF	ON	ON	OFF	OFF	ON	ON	
5	н	×	L	н	L	н	н	ON	OFF	ON	ON	OFF	ON	ON	İ
6	н	×	L	н	н	L	н	ON	OFF	ON	ON	QN	ON	ON	
7	H	х	L	н	н	Н	н	ON	ON	ON	OFF	OFF	OFF	OFF	
8	Н	Х	Н	L	L	L	Н	ON	ON	ON	ON	ON	ON	ON	1
9	н	×	Н	L	L	H	н	ON	ON	ON	ON	OFF	ON	ON	
10	н	×	Н	L	н	L	н	OFF	OFF	OFF	ON	ON	OFF	ON	
11	н	х	Н	L	н	н	н	OFF	OFF	ON	ON	OFF	OFF	ON	
12	н	Х	Н	Н	L	L	Н	OFF	ON	OFF	OFF	OFF	ON	OΝ	
13	Н	×	Н	Н	L	н	н	ON	OFF	OFF	ON	OFF	ON	ON	
14	н	x	Н	Н	Н	L	н	OFF	OFF	OFF	ON	ON	ON	ON	
15	н	х	н	Н	Н	_ н	Ŧ	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
हा	х	X	х	Х	X	Х	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	2
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3
<u>IT</u>	L	Х	Х	Х	Х	х	Н	ON	ON	ON	ON	ON	ON	ON	4

'LS248 FUNCTION TABLE (T2)

DECIMAL OR			INP	UTS			BI/RBQ†	•		0	UTPU	TS			NOTE
FUNCTION	LT	RBI	D	С	8	Α		а	ь	c	d	e	f	g	
0	н	н	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	L	
1	н	×	L	L	L	Н	н	L.	H	H	L	Ļ	L	L	
2	Н	×	L	L	Н	L	Н	н	Н	L	Н	Н	L	Н	
3	Н	х	L	L	Н	_ H	н	Н	Н	H	H	L	L	H	
4	Н	Х	L	Н	L	L	н	L	Н	Н	L	L	Н	Н	
5	Н	х	L	Н	L	H	н	H	L	Н	Н	L	Н	Н	
6	н	х	L	Н	Н	L	н	н	L	Н	Н	н	Н	н	
7	H	х	L	н	Н	н	н	н	Н	Н	L	L	L	L	1
8	Н	Х	Н	L	L	L	Н	H	Н	Н	Н	Н	Н	I	•
9	н	X	H	L	L	Н	н	Н	H	H	H	L	Н	н	
10	Н	X	Н	L	Н	L	Н	Ł	L	L	Н	Н	L	н	
11	Н	х	H	L	Н	Н	н	L	L	н	н	L	L	H	
12	I	Х	Н	Н	Ļ	L	Н	L	Н	Ĺ	L	L	Н	Н	
13	Н	X	Н	Н	L	Н	Н	Н	L	L	H	L	Н	н	
14	Н	х	Н	Н	Н	L	н	L	L	L	Н	н	Н	н	İ
15	н	×	н	Н	Н	н	н	L	L	L	L	L	L	L	
BI	Х	×	Х	Х	Х	Х	Ĺ	L	L	L	L	L	L	L	2
RBI	н	L	L	L	L	L	L	L	L	L	Ļ	L	L	ᆸ	3
LT	L	X	Х	Х	Х	X	н	Н	Н	н	H	Н	Н	н	4

H = high level, L = low level, X = irrelevant

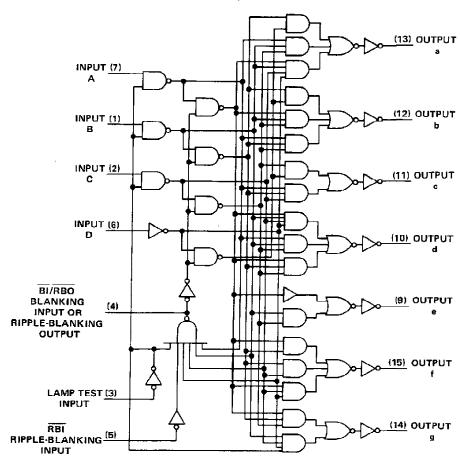
- NOTES: 1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.
 - 2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are low regardless of the level of any other input.
 - 3. When ripple-blanking input (RBI) and Inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go low and the ripple-blanking output (RBO) goes to a low level (response condition).
 - When the blanking input/ripple-blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are high.

 $^{\dagger}\overline{BI/RBO}$ is wire-AND logic serving as blanking input (\$\overline{BI}\$) and/or ripple-blanking output (\$\overline{RBO}\$).



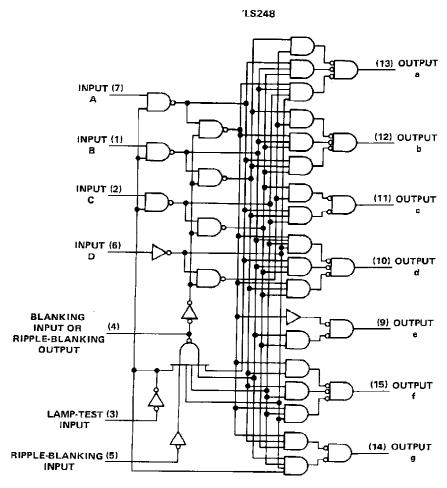
logic diagram (positive logic)

'246, '247, 'LS247



Pin numbers shown are for D, J, N, and W packages.

logic diagram (positive logic)

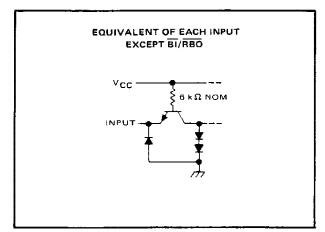


Pin numbers shown are for D, J, N, and W packages.

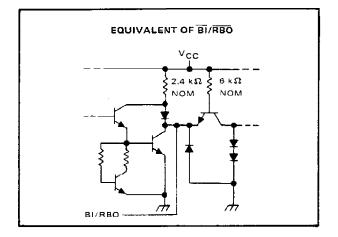
SN54246, SN54247, SN74246, SN74247 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

schematics of inputs and outputs

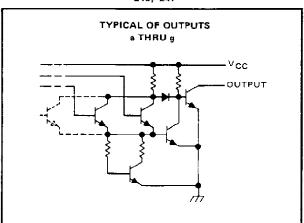
'246, '247



'246, '247



'246, '247

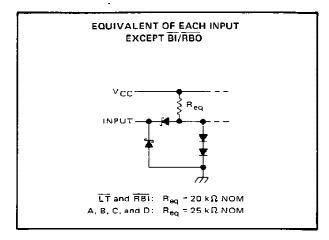


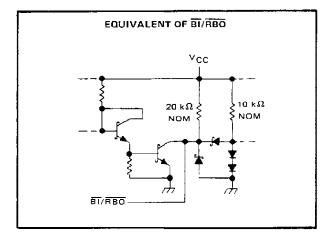
SN54LS247, SN54LS248, SN74LS247, SN74LS248 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

schematics of inputs and outputs

'LS247, 'LS248

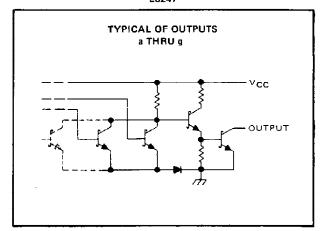
'LS247, 'LS248

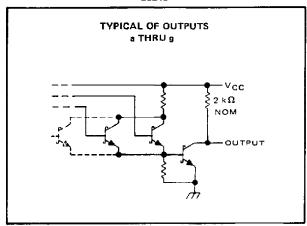




'LS247

'LS248





SN54246, SN54247, SN74246, SN74247 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

Supply voltage, VCC (see Note 1) .																7
Input voltage									_							5.5
Current forced into any output in the	off sta	te				 -			_							1 m
Operating free-air temperature range:	SN542	46,	SN	5424	17						_		_£	ن5° (C to	125°
•	SN742	46,	SN	7424	17			 _						0	°C t	o 70°
Storage temperature range												_	-6	i5° (C to	150°

recommended operating conditions

			SN5424	6		N5424	7		SN7424	6] :	N7424	7	
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Supply voltage, VCC		4.5	5	5.5	4.5	5	5.5	4.75	5	5.25	4.75	5	5.25	ν
Off-state output voltage, VO(off)	a thru g	Ţ		30			15			30			15	٧
On-state output current, IO(on)	a thru g			40			40			40			40	mΑ
High-level output current, IOH	BI/RBO	ŀ		-200		-	-200			-200			200	μА
Low-level output current, IOL	BI/RBO	•		8			8			8			8	mA
Operating free-air temperature, T _A	1	-55		125	-55		125	0		70	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		TEST CONDITIONS†	MIN	TYPI	MAX	UNIT
ViH	High-level input voltage			2			٧
VIL	Low-level input voltage					0.8	ν
Vik	Input clamp voltage		V _{CC} = MIN, I ₁ = -12 mA			1.5 V	٧
Voн	High-level output voltage	BI/RBÓ	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -200 μA	2.4	3.7		٧
VOL	Low-level output voltage	BĪ/RBŌ	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 8 mA		0.27	0.4	٧
O(off)	Off-state output current	a thru g	V _{CC} = MAX, V _H = 2 V, V _{IL} = 0.8 V. V _{O(off)} = MAX			250	μА
VO(on)	On-state output voltage	a thru g	$V_{CC} = MIN, V_{IH} = 2V,$ $V_{IL} = 0.8 V, I_{O(an)} = 40 \text{ mA}$		0.3	0.4	v
l _j	Input current at maximum input voltage	Any input except BI/RBO	V _{CC} = MAX, V _I = 5.5 V			1	mA
ЧН	High-level input current	Any input except BI/R80	V _{CC} = MAX, V ₁ = 2.4 V			40	μΑ
l _i L	Low-level input current	Any input except BI/RBO BI/RBO	V _{CC} = MAX, V ₁ = 0.4 V			-1.6 -4	mA
los	Short-circuit output current	BI/RBO	V _{CC} = MAX			-4	mA
Icc	Supply current	'	V _{CC} = MAX, See Note 2		64	103	mΑ

 $^{^{\}dagger}$ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ} \text{ C}$

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
toff	Turn-off time from A input				100	
ton	Turn-on time from A input	CL = 15 pF, RL = 120 Ω,			100	n s
toff	Turn-off time from RBI input	See Note 3			100	
ton	Turn-on time from RBI input				100	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



 $[\]ddagger$ All typical values are at $V_{CC} = 5 \text{ V. } T_{A} = 25^{\circ}\text{C.}$

NOTE 2: $f_{\mbox{CC}}$ is measured with all outputs open and all inputs at 4.5 V.

solute maximum ratings over operating free-air t	em	pe	ra	tur	e	rar	nge) (un	les	s (oth	ıeı	rw	ise	n	oŧ	ed	1)				
Supply voltage, VCC (see Note 1)																							. 7
Input voltage																							. 7
Peak output current (t _W ≤ 1 ms, duty cycle ≤ 10%)																							200 m
Current forced into any output in the off state																						-	. 1 m/
Operating free-air temperature range: SN54LS247																				-5	5°	C t	to 125°
SN74LS247																					C)°C	to 70°
Storage temperature range																							
E 1: Voltage values are with respect to network ground termin																							

recommended operating conditions

		SI	V54LS2	47	SI	174LS2	47	UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	ויייטן
Supply voltage, V _{CC}		4.5	5	5.5	4.75	5	5.25	V
Off-state output voltage, VO(off)	a thru g			15			15	٧
On-state output current, IO(on)	a thru g			12			24	mΑ
High-level output current, IOH	BT/RBO			-50			-50	μА
Low-level output current, IOL	BT/RBO			1.6			3.2	mΑ
Operating free-air temperature, TA		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

			7507.001	t	SI	N54LS2	47	Sf	V74LS2	47	UNIT
	PARAMETER		I IEST CON	IDITIONS†	MIN	TYP‡	MAX	MIN	TYPİ	MAX	UNIT
VIH	High-level input voltage	-		•	2			2			V
VIL	Low-level input voltage				<u> </u>		0.7			8.0	V
VIK	Input clamp voltage		VCC = MIN,	I _I = -18 mA			-1.5			-1.5	٧
VoH	High-level output voltage	BI/RBO	V _{CC} = MIN, V _{IL} = V _{IL} max,	V _{IH} = 2 V, I _{OH} = -50 μA	2.4	4.2		2.4	4.2		٧
VOL	Low-level output voltage	BI/RBO	V _{CC} = MIN, V _{IH} = 2 V,	IOL = 1.6 mA		0.25	0.4		0.25	0.4	V
VOL	LOW-level output voltage	BITTE	VIL = VIL max	IOL = 3.2 mA	_				0.35	0.5	_
IO(off)	Off-state output current	a thru g	V _{CC} = MAX, V _{IL} = V _{IL} max,	V _{IH} = 2 V, V _{O(off)} = 15 V			250			250	μД
Va.	On-state output voltage	a thru q	V _{CC} = MIN, V _{IH} = 2 V,	I _{O(on)} = 12 mA		0.25	0.4		0.25	0.4	V
VO(on)	On-state output voitage	a wina g	V _{IL} = V _{IL} max	I _{O(on)} = 24 mA					0.35	0.5	
Ϊį	Input current at maximur	n input voltage	VCC = MAX,	V ₁ = 7 V			0.1			0.1	mA
TIH	High-level input current	· · · · · · · · · · · · · · · · · · ·	VCC = MAX.	V ₁ = 2.7 V			20			20	μА
I _{IL}	Low-level input current	Any input except BI/RBO	V _{CC} = MAX,	V1 = 0.4 V			-0.4			-0.4	mA
		BI/RBO					-1.2			-1.2	
los	Short-circuit output current	BI/RBO	V _{CC} = MAX		-0.3		2	0.3		-2	πА
lcc	Supply current		V _{CC} = MAX,	See Note 2		7	13		7	13	mA

 $^{^\}dagger$ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics, VCC = 5 V, T_A = 25° C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	TINU
toff	Turn-off time from A input				100	ns
ton	Turn-on time from A input	$C_{L} = 15 pF, R_{L} = 665 \Omega,$			100	115
toff	Turn-off time from RBI input	See Note 3			100	
ton	Turn-on time from RBI input				100	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

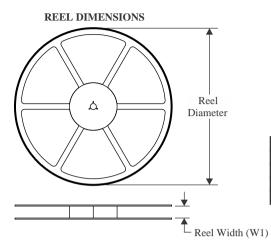


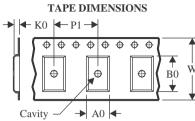
 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C. NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

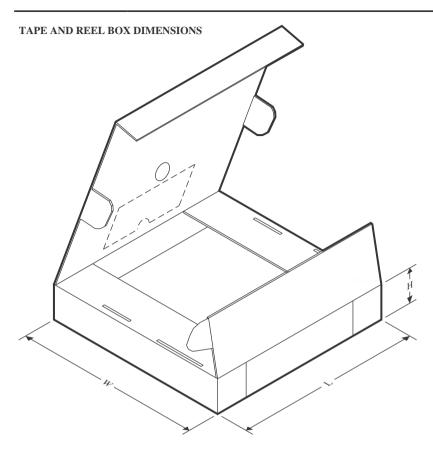


*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS247DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LS247NSR	so	NS	16	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1

PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

	Device	Device Package Type		Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
I	SN74LS247DR	SOIC	D	16	2500	340.5	336.1	32.0	
ſ	SN74LS247NSR	SO	NS	16	2000	367.0	367.0	38.0	

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

7 III dilitorio di Carta i i citti i di									
Device	evice Package Name		Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)	
SN74LS247D	D	SOIC	16	40	507	8	3940	4.32	
SN74LS247N	N	PDIP	16	25	506	13.97	11230	4.32	
SN74LS247N	N	PDIP	16	25	506	13.97	11230	4.32	
SN74LS247NE4	N	PDIP	16	25	506	13.97	11230	4.32	
SN74LS247NE4	N	PDIP	16	25	506	13.97	11230	4.32	

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