TPS2400 Overvoltage Protection Controller

1 Features

- Up to 100-V Overvoltage Protection
- 6.9-V Overvoltage Shutdown Threshold
- 3-V Undervoltage Shutdown Threshold
- Overvoltage Turnoff Time Less than 1 µs
- External N-Channel MOSFET Driven by Internal Charge Pump
- 1-mA Maximum Static Supply Current
- 5-Pin SOT−23 Package
- −40°C to 85°C Ambient Temperature Range
- 2.5-kV Human-Body-Model, 500-V CDM Electrostatic Discharge Protection

2 Applications

- Cellular Phones
- PDAs
- Portable PCs
- Media Players
- Digital Cameras
- GPS

3 Description

The TPS2400 overvoltage protection controller is used with an external N-channel MOSFET to isolate sensitive electronics from destructive voltage spikes and surges. It is specifically designed to prevent large voltage transients associated with automotive environments (load dump) from damaging sensitive circuitry. When potentially damaging voltage levels are detected by the TPS2400 the supply is disconnected from the load before any damage can occur.

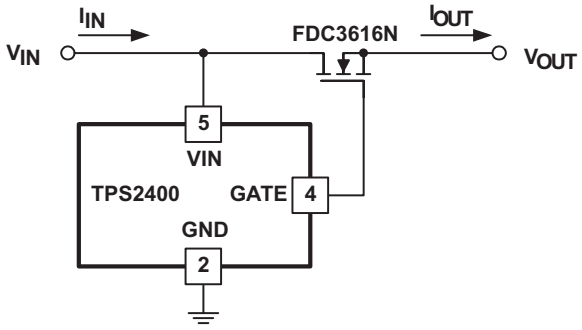
Internal circuitry includes a trimmed band-gap reference, oscillator, Zener diode, charge pump, comparator, and control logic. The TPS2400 device is designed for use with an external N-channel MOSFET, which are readily available in a wide variety of voltages.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS2400	SOT-23 (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Application Diagram



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4 Revision History

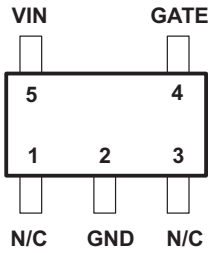
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (August 2008) to Revision B **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GATE	4	O	Output gate drive for an external N-channel MOSFET
GND	2	—	Ground
NC	1, 3	—	No internal connection
VIN	5	I	Input voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{VIN}	Input voltage	VIN	–0.3	110	V
V_{OUT}	Output voltage	GATE (continuous)	–0.3	22	V
		GATE (transient, < 10 µs, Duty Cycle < 0.1%)	–0.3	25	
	Continuous total power dissipation		See *Thermal Information*		
T_J	Operating junction temperature		–40	125	°C
T_A	Operating free-air temperature		–40	85	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage at V_{IN}	3.1		6.8	V
Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC (1)		TPS2400 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	219.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	126.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	15.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	50.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
$I_{I(VIN)}$	Input supply current, V_{IN}	$V_{I(VIN)}$ = 3.1 V		65	110	µA
		$V_{I(VIN)}$ = 5 V		95	180	
		$V_{I(VIN)}$ = 6.5 V		135	220	
		$V_{I(VIN)}$ = 100 V		550	1000	
$UVLO_{(upper)}$	Undervoltage lockout upper threshold	$V_{I(VIN)}$ rising	2.9	3	3.1	V
$UVLO_{(hyst)}$	Undervoltage lockout hysteresis		85	100	115	mV
$OVP_{(upper)}$	Overvoltage protection upper threshold	$V_{I(VIN)}$) rising	6.7	6.9	7.1	V
$OVP_{(hyst)}$	Overvoltage protection hysteresis		135	150	165	mV
GATE DRIVE						
$I_{OSOURCE(gate)}$	Gate sourcing current	$V_{I(VIN)}$ = 3.1 V, $V_{O(gate)}$ = 7 V	3		10	µA
		$V_{I(VIN)}$ = 5 V, $V_{O(gate)}$ = 10 V	3		10	
$I_{OSINK(gate)}$	Gate sinking current(1)	$V_{I(VIN)}$ = 7.2 V, $V_{O(gate)}$ = 15 V	350	485	600	mA
$V_{OH(gate)}$	Gate output high voltage	$V_{I(VIN)}$ = 3.1 V, $I_{OSOURCE(gate)}$ = 1 µA	10		12	V
		$V_{I(VIN)}$ = 5 V, $I_{OSOURCE(gate}$) = 1.5 µA	16		19	
		$V_{I(VIN)}$ = 6.5 V, $I_{OSOURCE(gate)}$ = 1.5 µA	16		20	
$V_{OHMAX(gate)}$	Gate output high maximum voltage	$I_{OSOURCE(gate)}$ = 0 µA			20	V
$V_{OL(gate)}$	Gate output low voltage	$V_{I(VIN)}$ = 7.2 V, $I_{OSINK(gate)}$ = 50 mA			1	V
$T_{ON(prop)}$	Gate turnon propogation delay, (50% $V_{I(vin)}$ to $V_{O(gate)}$ = 1 V, R_{LOAD} = 10 MΩ	$V_{I(VIN)}$ stepped from 0 V to 5 V, C_{LOAD} = 1 nF	0.1		0.6	ms
		C_{LOAD} = 10 nF	0.9		3	
$T_{ON(rise)}$	Gate turnon rise time, ($V_{O(gate)}$ = 1 V to 90%$V_{O(gate)}$, R_{LOAD} = 10 MΩ)	$V_{I(VIN)}$ stepped from 0 V to 5 V, C_{LOAD} = 1 nF	1.5		6	ms
		C_{LOAD} = 10 nF	15		55	
T_{OFF}	Turnoff time, (50% $V_{I(VIN)}$ step to $V_{O(GATE)}$ = 6.9 V, R_{LOAD} = 10 MΩ)	$V_{I(VIN)}$ stepped from 6 V to 8 V, C_{LOAD} = 1 nF	5		0.25	µs
		C_{LOAD} = 10 nF	5		0.5	

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

6.6 Typical Characteristics

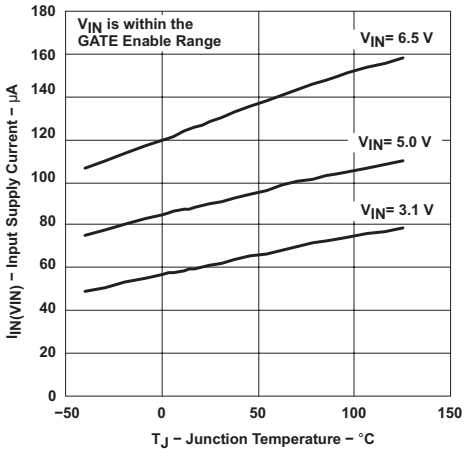


Figure 1. Input Supply current vs Junction Temperature

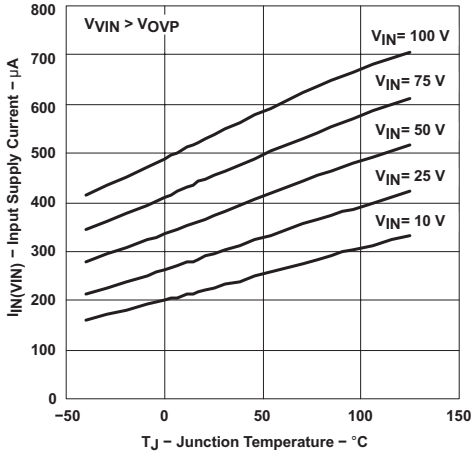


Figure 2. Input Supply current vs Junction Temperature

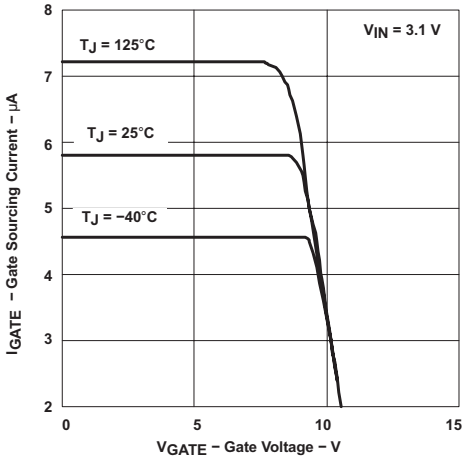


Figure 3. Gate Sourcing Current vs Gate Voltage

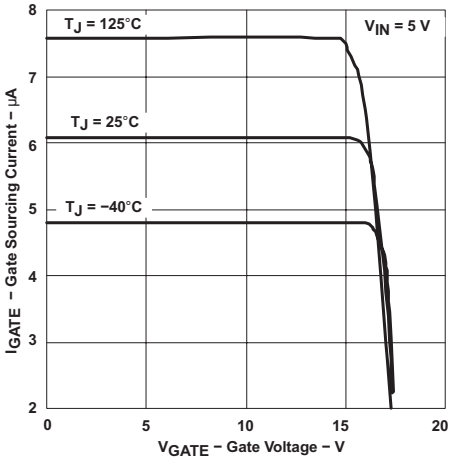


Figure 4. Gate Sourcing Current vs Gate Voltage

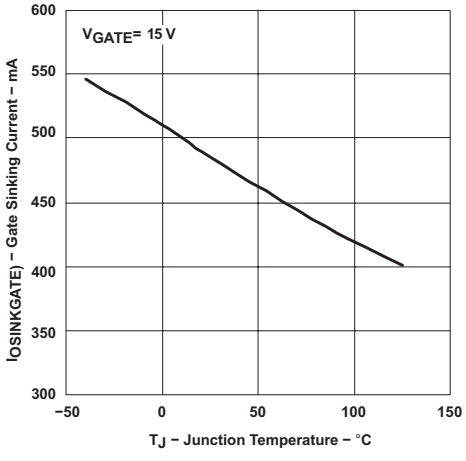


Figure 5. Gate Sinking Current vs Junction Temperature

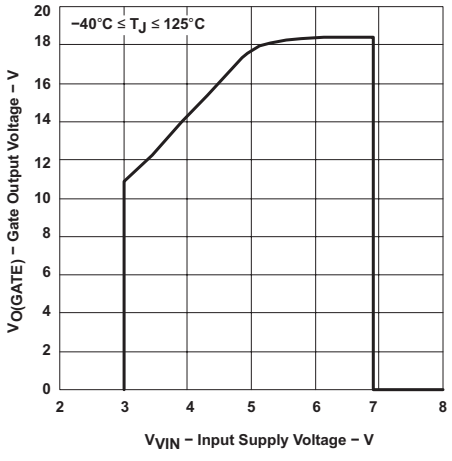


Figure 6. Gate Output Voltage vs Input Supply Voltage

Typical Characteristics (continued)

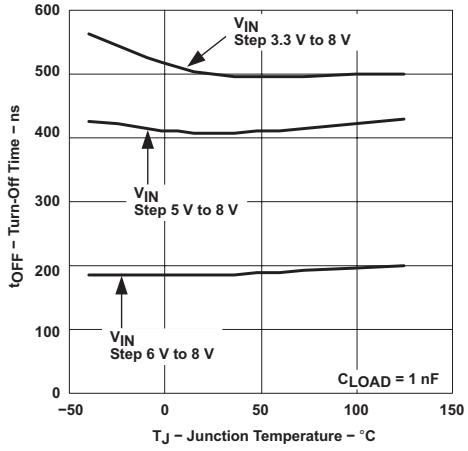


Figure 7. Turnoff Time to V_{GATE} = 6.9 V vs Junction Temperature

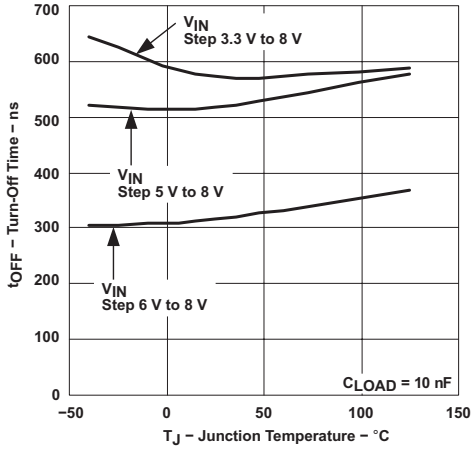


Figure 8. Turnoff Time to V_{GATE} = 6.9 V vs Junction Temperature

7 Parameter Measurement Information

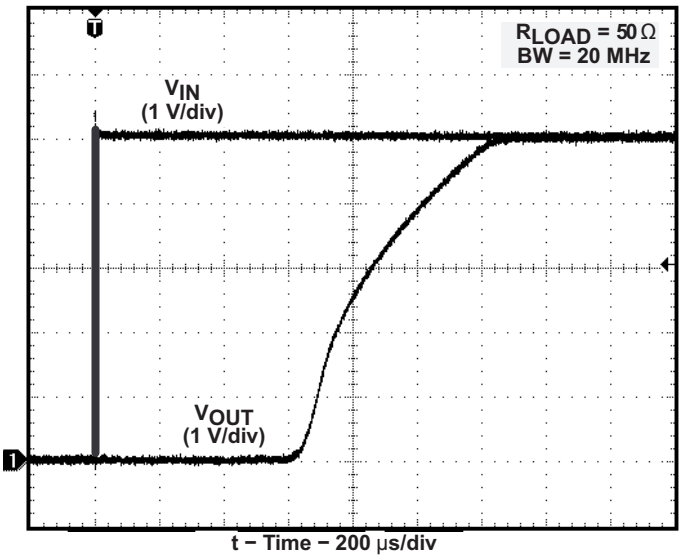


Figure 9. Output Turnon Response

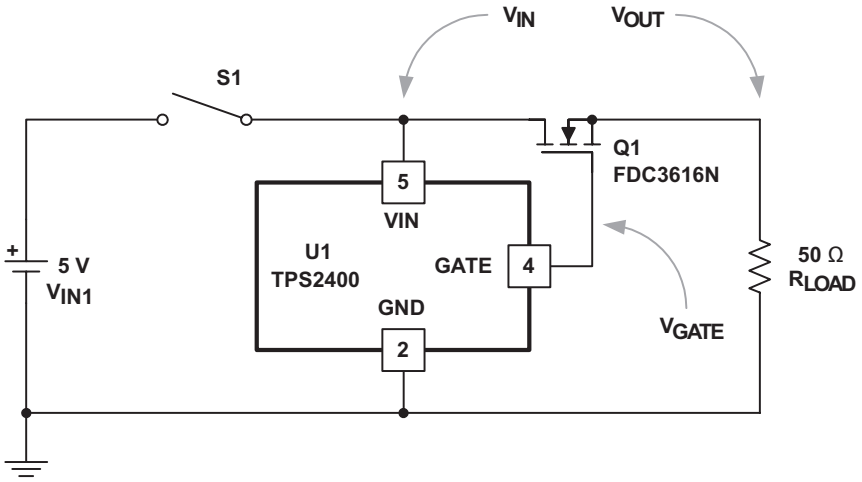


Figure 10. Output Turnon Response Test Circuit

Parameter Measurement Information (continued)

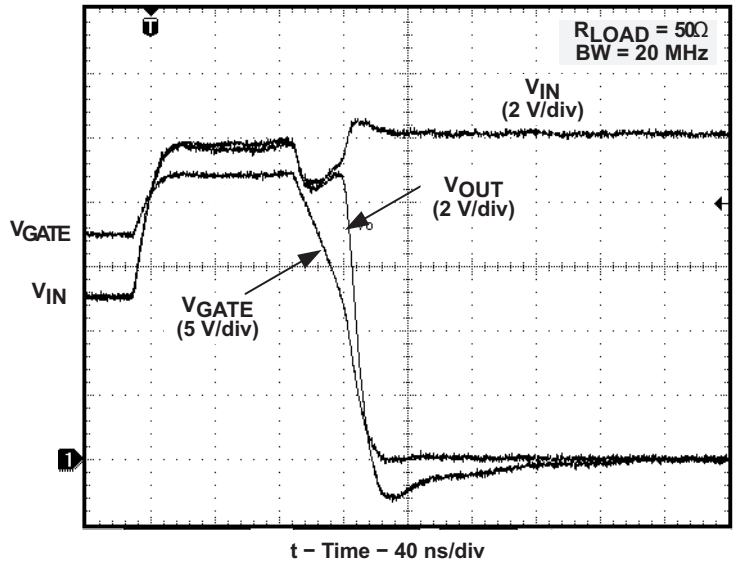


Figure 11. Output Turnoff Response

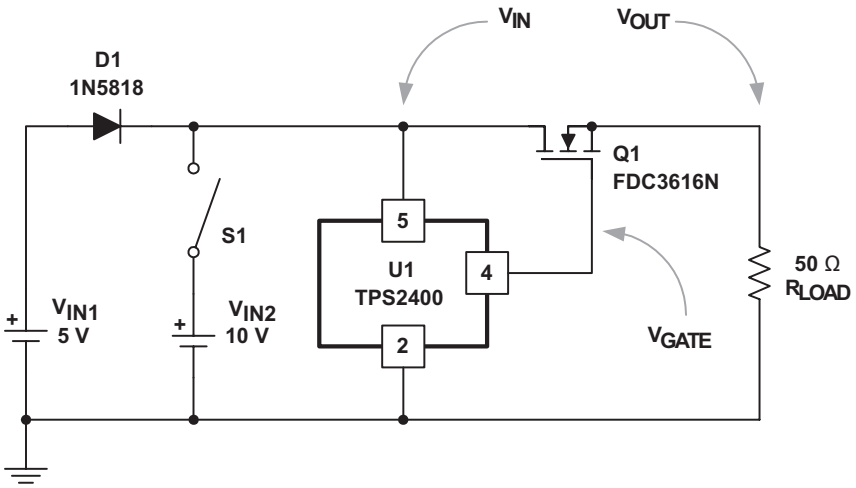


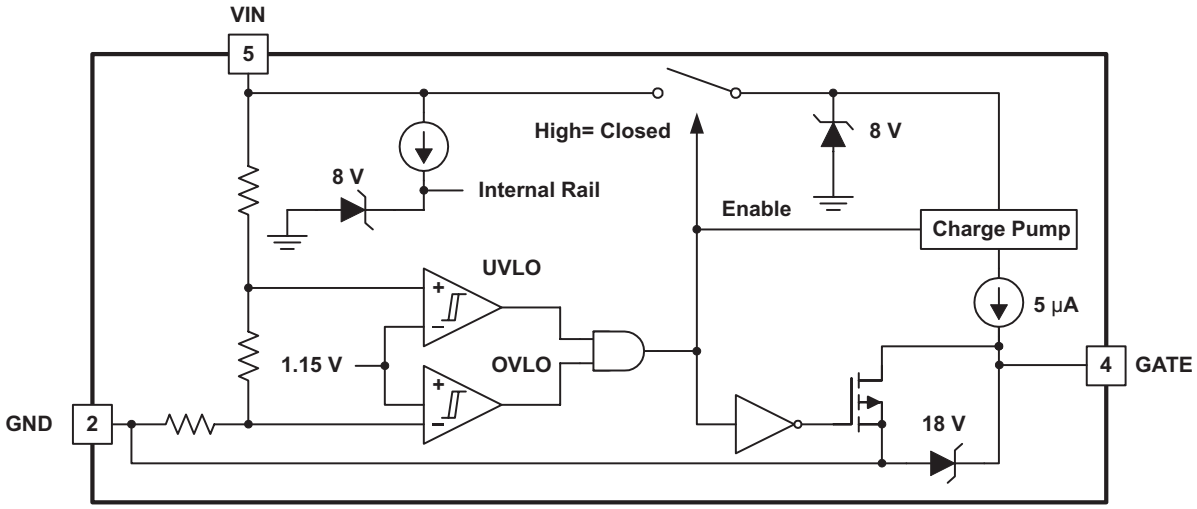
Figure 12. Output Turnoff Response Test Circuit

8 Detailed Description

8.1 Overview

The TPS2400 device is used in applications that must protect the load from overvoltage event. Benefits include fast response time and survival during extended overvoltage events.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Undervoltage and Overvoltage Comparators and Logic

When the comparators detect that VCC is within the operating window, the GATE output is driven high to turn on the external N-channel MOSFET. When V_{CC} goes above the set overvoltage level, or below the set undervoltage level, the GATE output is driven low.

8.3.2 Charge Pump

An internal charge pump supplies power to the GATE drive circuit and provides the necessary voltage to pull the gate of the MOSFET above the source.

8.3.3 Zener Diodes

Limit internal power rails to 8 V and GATE output to 18 V.

8.3.4 Shut-Off MOSFET

When an undervoltage or overvoltage event occurs, this MOSFET is turned on to pulldown the gate of the external N-channel MOSFET, thus isolating the load from the incoming transient.

Feature Description (continued)

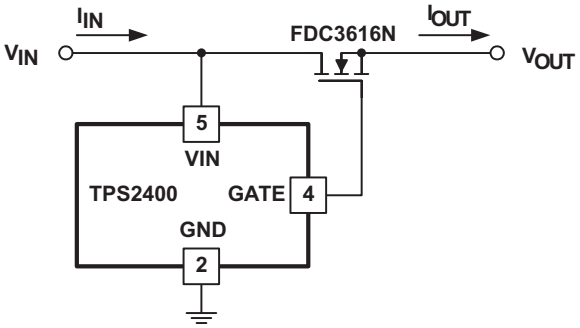


Figure 13. Application Diagram

8.4 Device Functional Modes

8.4.1 Overvoltage Protection

An overvoltage condition is commonly created in these situations:

- Unplugging a wall adapter from an AC outlet. Energy stored in the transformer magnetizing inductance is released and spikes the output voltage.
- Powering an appliance with the wrong voltage adapter (user error).
- Automotive load dump due to ignition, power windows, or starter motor (for example).
- An AC power-line transient.
- Power switch contact bounce (causes power supply/distribution inductive kick), (See Figure 14).

Many electronic appliances use a transient voltage suppressor (TVS) for overvoltage protection as shown in Figure 14. The TVS is typically a metal-oxide varister (MOV) or Transzorb. The former is a nonlinear resistor with a soft turnon characteristic whereas the latter is a large junction Zener diode with a very sharp turnon characteristic. These devices have high pulse-power capability and pico-second response time. A TVS clamps the load voltage to a safe level so the load operates uninterrupted in the presence of power supply output-voltage spikes. But in the event of a voltage surge, fuse F2 blows and must be replaced to restore operation.

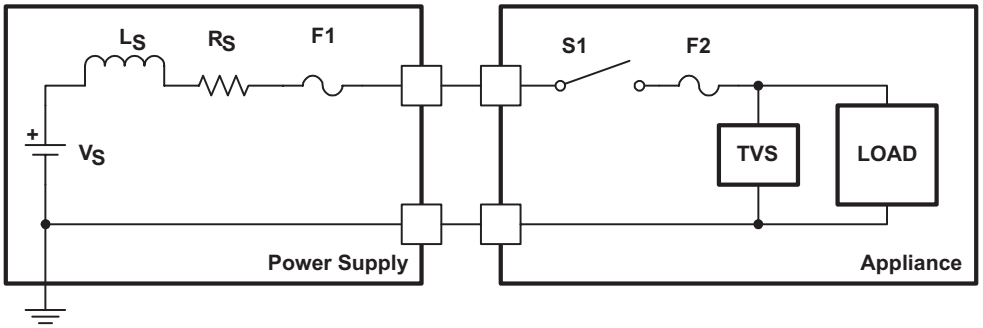


Figure 14. Load Protection Using Transient Voltage Suppressor Clamps

The TPS2400 circuit in Figure 15 protects the load from an overvoltage, not by clamping the load voltage like a TVS, but by disconnecting the load from the power supply. The circuit responds to an overvoltage in less than 1 µs and rides out a voltage surge without blowing fuse F2. The voltage surge can be of indefinite duration.

The load can see a voltage spike of up to 1 µs, the amount of time it takes the TPS2400 to disconnect the load from the power supply. A low-power Zener diode D2 can be used to clamp the load voltage to a safe level. In most cases, diode D2 is not necessary because the load bypass capacitor (not shown) forms a low-pass filter with resistor R_S and inductor L_S to significantly attenuate the spike.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS2400 device provides application flexibility and can be used in many types of systems for load protection.

9.2 Typical Applications

9.2.1 TPS2400 Application

When the TPS2400 disconnects the load from the power supply, the power-supply output-voltage spikes as the stored energy in inductor LS is released. A Zener diode D1 or a small ceramic capacitor can be used to keep the voltage spike at a safe level.

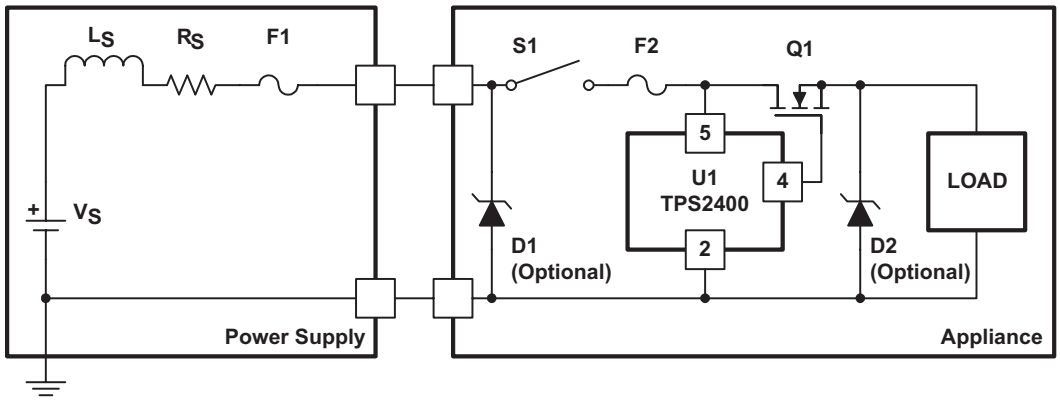


Figure 15. TPS2400 Application Block Diagram

9.2.1.1 Design Requirements

Table 1 shows the parameters for this design example.

Table 1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
MOSFET Input Capacitance, CG	2 nF
Load Capacitance, CL	100 uF

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Controlling the Load Inrush-Current

Figure 16 is a simplified representation of an appliance with a plug-in power supply (for example, wall adapter). When power is first applied to the load in Figure 16, the large filter capacitor C_{LOAD} acts like a short circuit, producing an immediate inrush-current that is limited by the power-supply output resistance and inductance, R_S and L_S, respectively. This current can be several orders of magnitude greater than the steady-state load current. The large inrush current can damage power connectors P1 and J1 and power switch S1, and stress components. Increasing the power-supply output resistance and inductance lowers the inrush current. However, the former increases system power-dissipation and the latter decreases connector and switch reliability by encouraging the contacts to arc when they bounce.

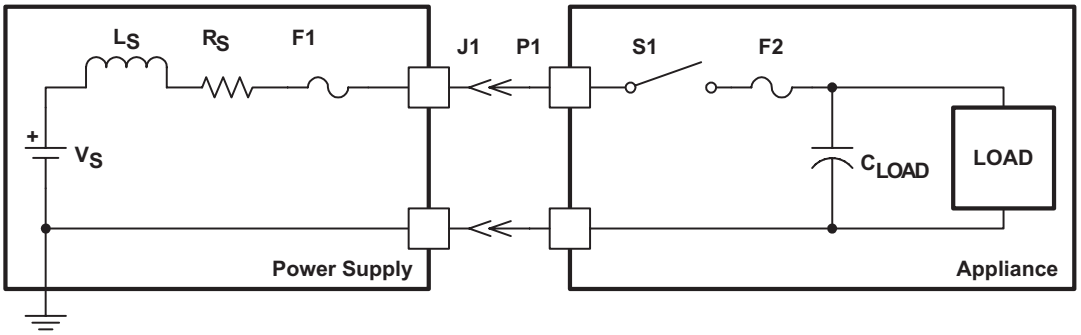


Figure 16. Power-Supply Output Resistance and Inductance Circuit Model

The TPS2400 circuit in Figure 17 limits the inrush current without these draw backs. The TPS2400 device charges the transistor Q1 gate capacitance CG with a 5-µA source when Q1 is commanded to turn on. Transistor Q1 is wired as a source follower so the gate-voltage slew rate and the load-voltage slew rate are identical and equal to

$$\frac{\partial V_L}{\partial t} = \frac{5\ \mu A}{C_G} \tag{1}$$

The corresponding inrush current is:

$$I_{INRUSH} \approx C_L \times \frac{\partial V_L}{\partial t} = \left(\frac{C_L}{C_G}\right) \times 5\ \mu A \tag{2}$$

When solving Equation 1 using CG = 2 nF, we get 2500 V/s. Then we can use Equation 2 to approximate the inrush current of 250 mA.

An external capacitor and a series 1-kΩ resistor can be connected to the gate of Q1 and ground to reduce inrush current further. In this case, the parameter CG in Equation 1 and Equation 2 is the sum of the internal and external FET gate capacitance. The 1-kΩ resistor decouples the external gate capacitor, so the TPS2400 device can rapidly turn off transistor Q1 in response to an overvoltage condition.

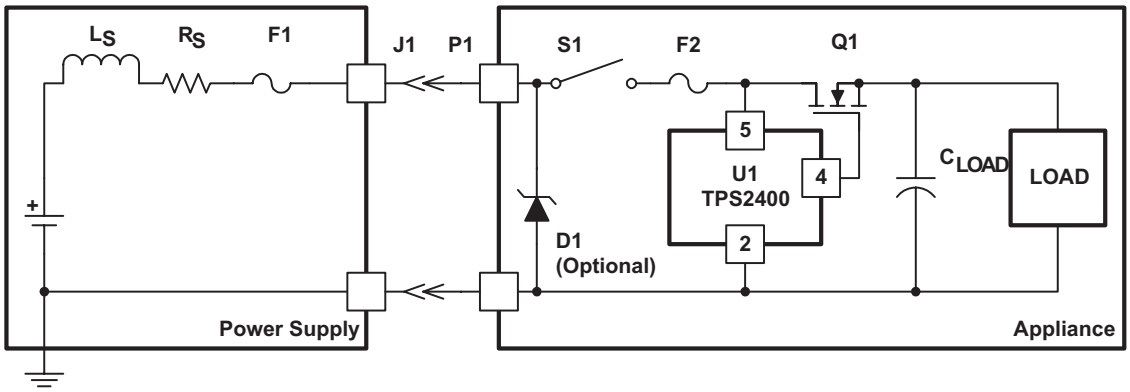


Figure 17. Turnon Voltage Slew Rate Control Using the TPS2400

9.2.1.3 Application Curve

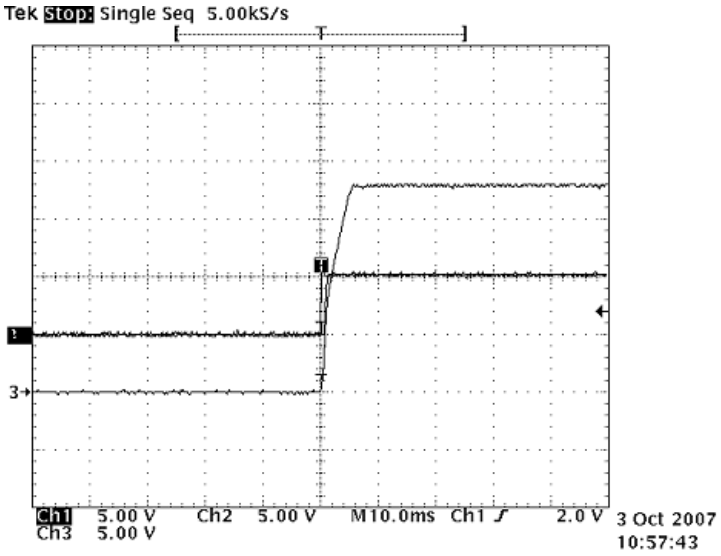


Figure 18. Circuit Start-Up With VIN = 5 V

9.2.2 High-Side Switch Overvoltage Protector That Can Drive a 12−V Load

Detailed information for the circuit shown in Figure 19 can be found in the application note, *Overvoltage Protector for High-Loads* (SLVA163).

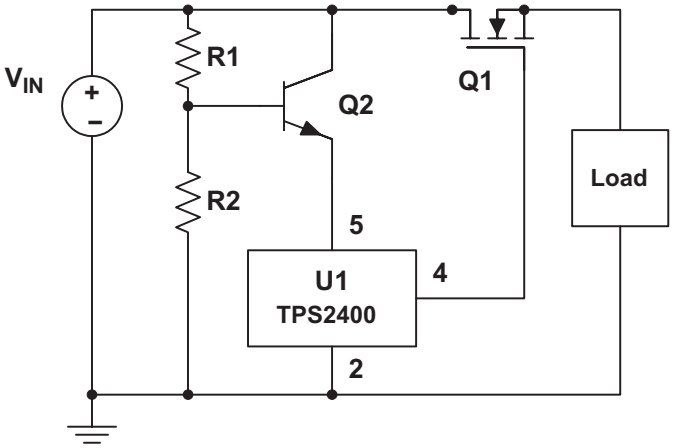


Figure 19. High-Side Switch Overvoltage Protector That Can Drive a 12−V Load

9.2.3 Low−Side Switch Overvoltage Protector That Can Drive a 12−V Load

Detailed information for the circuit shown in Figure 20 can be found in the application note, *Overvoltage Protector for High-Loads* (SLVA163).

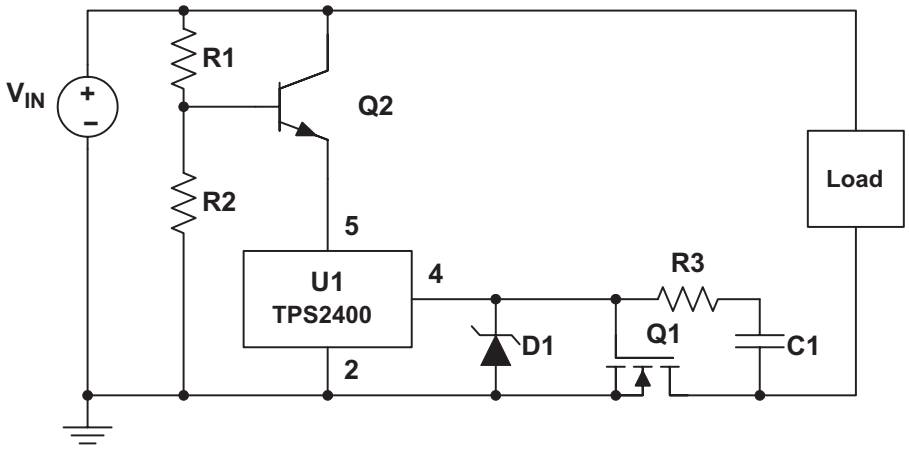


Figure 20. Low−Side Switch Overvoltage Protector That Can Drive a 12−V Load

10 Power Supply Recommendations

The TPS2400 device is designed to operate from 3.3-V to 5-V input supplies. VIN is 100-V tolerant, but keep within the recommended steady-state operating range of 3.1 V to 6.8 V.

11 Layout

11.1 Layout Guidelines

Parts placement must be driven by power flow in a point-to-point manner from input to output. Avoid leakage paths from GATE to GND, which might load down the small GATE output current.

11.2 Layout Example

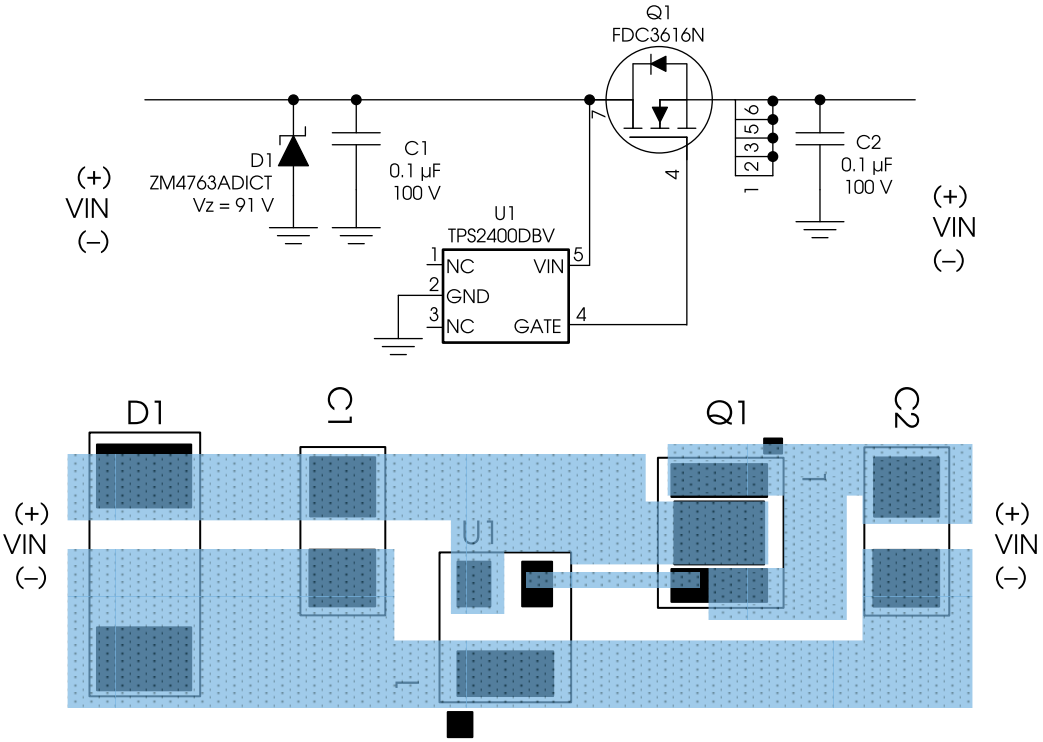


Figure 21. Suggested Layout

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

Overvoltage Protector for High−Voltage Loads, SLVA163.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2400DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BIJ	Samples
TPS2400DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BIJ	Samples
TPS2400DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BIJ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

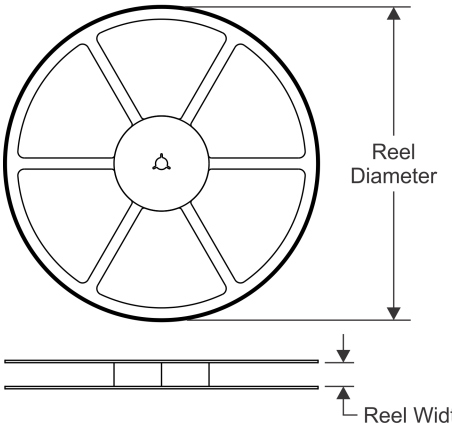
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

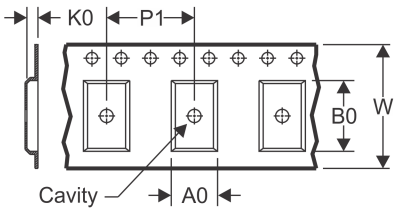
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

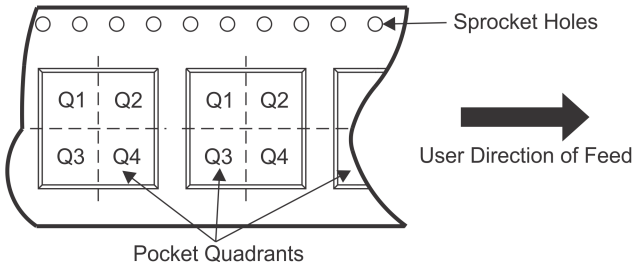


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

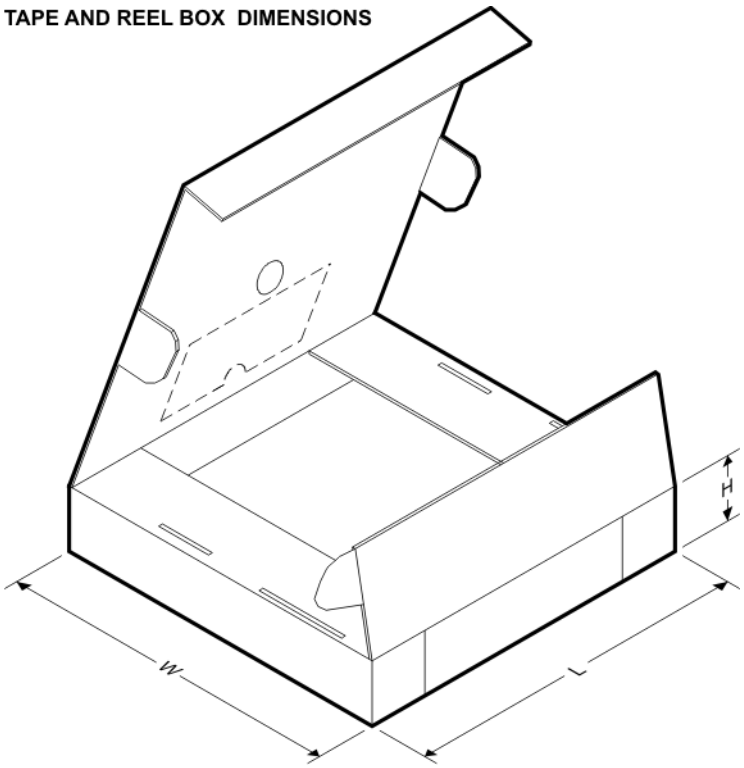
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2400DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS2400DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

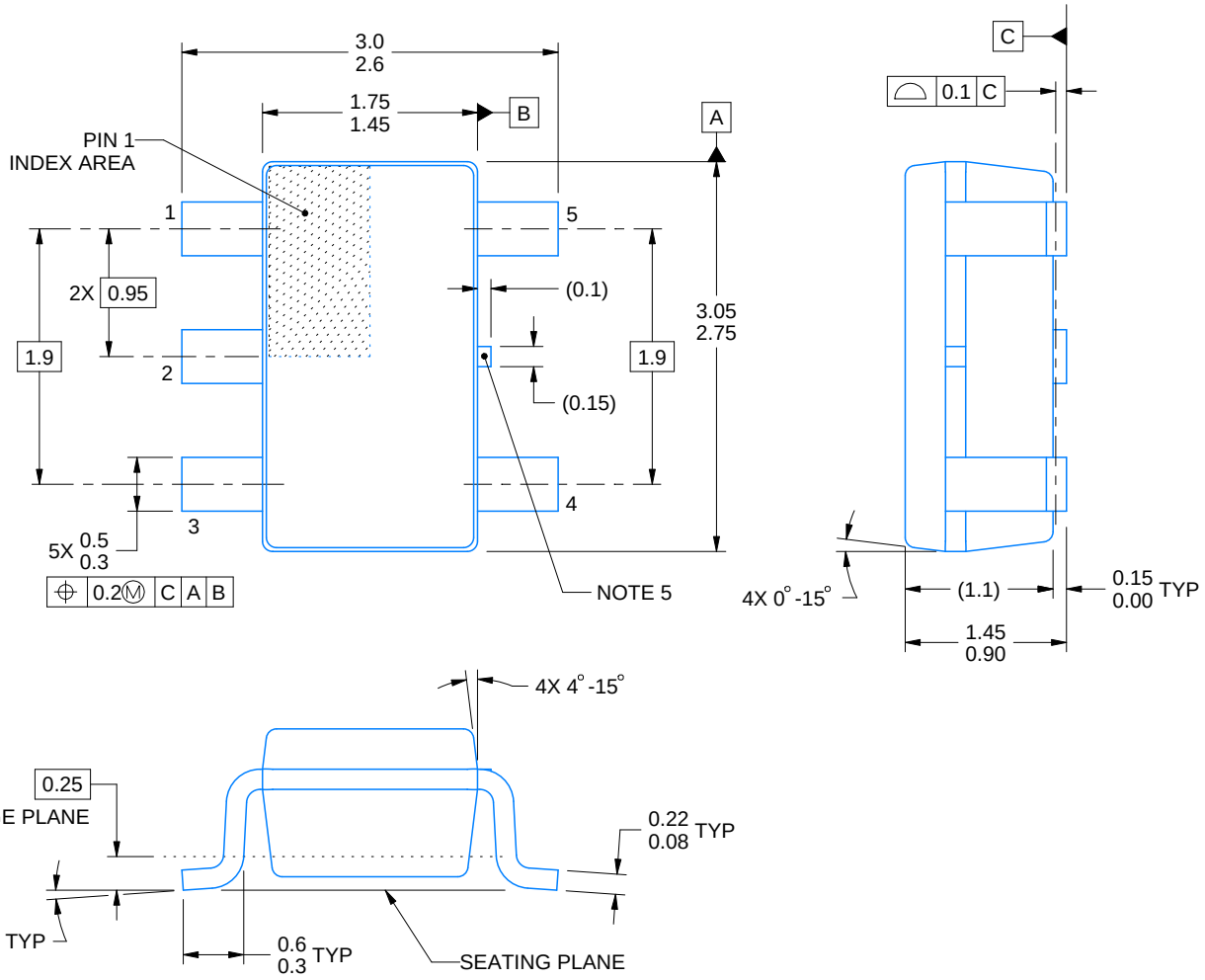
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2400DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS2400DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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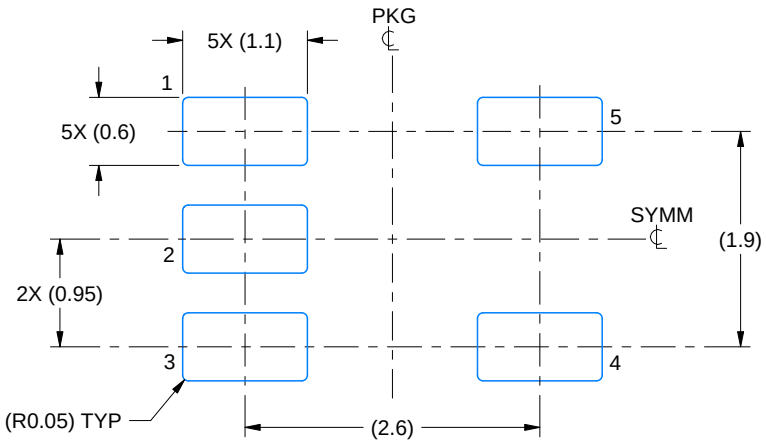
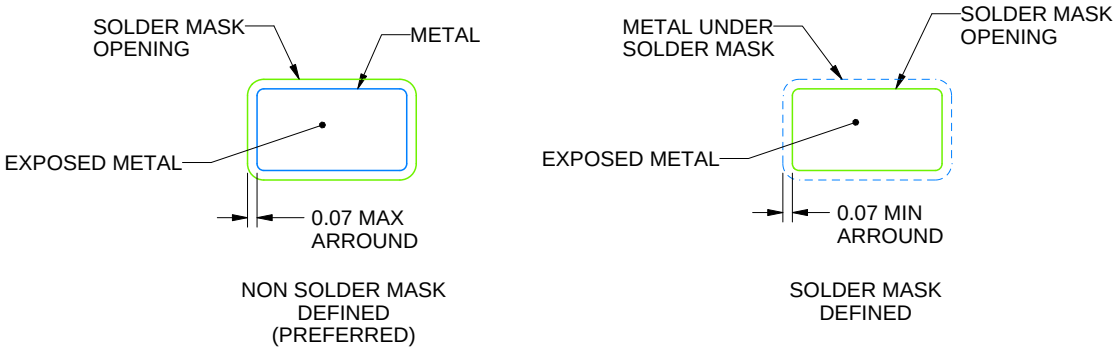
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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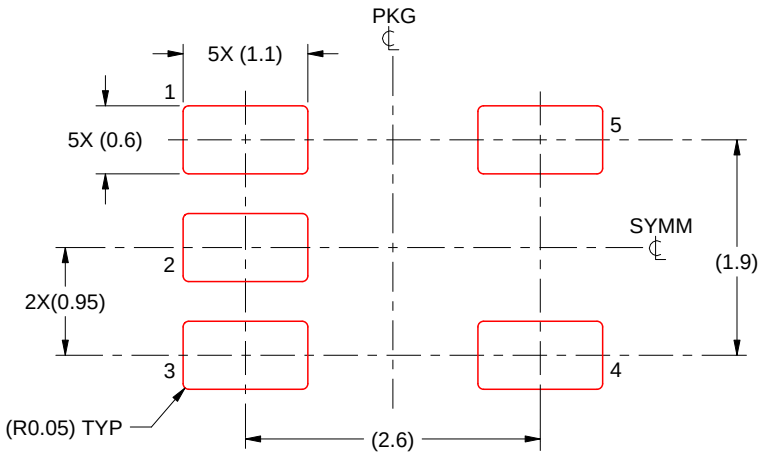
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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